In addition

$$\kappa = \frac{\epsilon - \epsilon_0}{\epsilon + \epsilon_0}.$$

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MSI High-Speed Low-Power GaAs Integrated Circuits Using Schottky Diode FET Logic

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***Abstract*—A new planar high-density (10^{-3} mm^2/gate) GaAs IC technology has been used for fabricating MSI digital circuits containing up to 75 gates/chip. These digital circuits have potential application for gigabit microwave data transmission and processor systems. The circuits consist of Schottky diode FET logic NOR gates, which have provided propagation delays in the 75–200-ps range with dynamic switching energies as low as 27 fJ/gate on ring oscillator structures. Power dissipation levels are compatible with future LSI/VLSI extensions. Operation of *D* flip-flops (*D*FF) as binary ripple dividers (÷2–÷8) was achieved at 1.9-GHz clock rates, and an 8:1 full-data multiplexer and 1:8 data demultiplexer were demonstrated at 1.1-GHz clock rates. This corresponds to equivalent propagation delays in the 100–175-ps range for these MSI circuits. Finally, a 3×3 parallel multiplier containing 75 gates functioned with a propagation delay of 172 ps/gate and with average gate power dissipations of as low as 0.42 mW/gate.**

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I. INTRODUCTION

THE SUCCESSFUL utilization of GaAs for digital integrated circuits has brought about higher speed and lower power logic circuits than were possible with silicon IC approaches. For example, GaAs frequency di-

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viders, designed for maximum speed, have been demonstrated at clock frequencies exceeding 4 GHz [2]. This will permit the development of frequency synthesizers well into the microwave range. Other digital circuits, such as multiplexers and demultiplexers, will also find application in gigabit microwave data transmission systems as they are implemented in high-speed GaAs versions and become more widely available. With development of high-speed comparators, latches, and sample–hold amplifiers, A/D converters having speeds that approach the microwave frequency range can be built. High-speed computational circuits such as multipliers, adders, memory devices, and GaAs CCD's will permit real-time digital signal processing functions to be carried out at gigabit data rates. Therefore, high-speed logic circuits are of interest to the microwave system community and will find many applications as the complexity and the availability of GaAs digital IC's increases.

While future system applications of gigabit digital circuits are possible at all levels of integration, an ever expanding range of applications will become available as complexity increases through the LSI range. This will allow such systems as microwave frequency synthesizers to be built on a single chip. In addition, it is desirable in high-speed integrated circuits to build at the highest possible level of integration, since off-chip interfacing through packages and transmission lines introduces propagation delay and is costly in power dissipation. Therefore, a competitive, practical, and versatile GaAs IC design should provide compatibility with LSI density and power requirements while maintaining propagation delays at least below 200 ps.

In this paper, an IC circuit design approach which fulfills these requirements will be described. This approach, referred to as Schottky Diode FET Logic (SDFL), utilizes small-area high-conductance ultra-low capacitance Schottky diodes to perform most logic functions. Inversion and current gain are obtained from depletion-mode (normally on) GaAs FET's with 1-μm gate length. Low-power dissipation (0.2–2 mW/gate) is obtained by utilizing low pinchoff voltage FET's (0.5–1.5 V). High gate densities (5×10^4–10^5/cm^2) are achieved by use of a planar fabrication process that employs multiple localized ion implantation, projection photolithography, and dry etching techniques. Details regarding the planar process have been published elsewhere [3], [4]. Logic gate propagation delays of 100 ps have been obtained, comparable to the performance previously reported on higher pinchoff voltage, depletion-mode GaAs FET IC's [2], but one to two orders of magnitude less power is required by the SDFL approach due to the lower pinchoff voltage and smaller channel widths. The above conditions will permit the extension of high-performance GaAs IC complexities into the LSI range, while maintaining high speed and sufficient noise margins (0.75–1 V).

The SDFL planar GaAs IC approach has been successful in the fabrication of MSI logic circuits with over 75 gates/chip. In the following sections, the SDFL circuit approach will be described and the high-speed performance of a three-stage frequency divider, an 8-channel data multiplexer, an 8-channel data demultiplexer, and a 3-bit parallel multiplier will be presented.

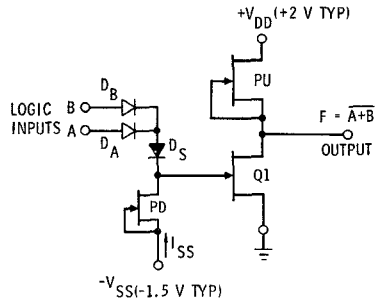

Fig. 1. Schematic of Schottky diode FET logic (SDFL) NOR gate.

II. Circuit Approach

The circuit diagram of a 2-input Schottky diode FET logic (SDFL) NOR gate is shown in Fig. 1. In this gate, the logical OR function is provided by the 1×2-μm Schottky diodes D_A and D_B which have junction capacitances of 2 fF and series resistances as low as 300 Ω. These diodes require a deep ($\sim$0.5-μm) low sheet-resistance implant for their fabrication, whereas the low-power high-transconductance GaAs MESFET's require a very shallow (0.1-μm) higher sheet-resistance implant. As a consequence, SDFL circuits cannot be fabricated by mesa-epitaxial or mesa-uniform implant fabrication techniques used for GaAs microwave FET's, but require two individual localized implants into the semi-insulating GaAs substrate. Input expansion is easily provided by additional logic diodes with little degradation in speed because of the extremely low reverse-bias diode capacitance. Small gate area is maintained, since the extremely small 2-terminal logic diodes require many fewer overcrossings than FET's or other 3-terminal active logic elements. These diodes also provide half of the level shifting required between drain and gate in depletion-mode logic. The pulldown active load (PD) provides the bias current for the logic diodes and most of the current required to turn off the gate of $Q1$. Fan-out of the basic NOR gate is limited to 3 or 4 by the ratio of PD and PU currents. However, fan-out expansion can easily be achieved, when necessary, by utilizing source followers or inverters as output buffers. Also, larger single NOR gates can be constructed for higher fanout requirements by scaling of FET channel widths. NOR gates composed of 5-, 8-, 10-, 15-, and 20-μm wide FET's have been fabricated and tested.

Ring oscillators, consisting of chains of odd numbers of logic gates, are used to evaluate propagation delay (τ_d) and dynamic switching energy ($P_D\tau_d$) of the SDFL logic gates. 5-μm NOR gates have yielded dynamic switching energies as low as 27 fJ/gate with 156-ps propagation delay, while 20-μm NOR gates have provided 75-ps propagation delay and 170-fJ/gate dynamic switching energy [1]. The speed and power are strongly influenced by gate width, pinchoff voltage, and gate layout area.

III. MSI Circuit Evaluation

While ring oscillators are useful devices for measurement of the basic speed–power properties of logic gates, a more realistic index of performance is provided by the operation of gates in real sequential or combinatorial logic circuits. In these circuits, high-speed performance is generally determined by worst case gate delay, using gates with average fan-ins and fan-outs of 2 to 3. For this study, the D flip-flop (DFF) was chosen as a representative example of sequential logic circuits because of its general usefulness in frequency dividers, counters, and data latches. A parallel multiplier, implemented with half and full adders, was selected as a combinatorial logic circuit example. These circuits fall within the MSI range of complexity (approximately 20–100 gates). All high-speed measurements required for testing these circuits have been made at wafer probe level. Output buffers (source followers) are located on-chip to prevent loading of the circuit during testing.

Binary ripple counters or frequency dividers have been made using the DFF as a basic building block. The DFF contains 6 NOR gates, interconnected to form 3 set-reset latches. By connecting the D (data) input to the $\bar{Q}$ output, the clock input will produce an output transition for every full clock cycle. Thus, each DFF stage divides by 2. The propagation delay per gate can be inferred from the maximum experimentally observed toggle frequency when compared with the results of a logic analysis modeling program. The program indicates that correct operation should be maintained up to $f_c = 1/(4.85\,\tau_d)$, where τ_d is the maximum propagation delay for a logic gate in the circuit.

Three stage dividers ($\div 8$) containing 25 NOR gates have been fabricated and have operated up to a clock frequency of 1.9 GHz. Fig. 2 shows the $\div 8$ output at 237 MHz from this divider. This corresponds to an equivalent propagation delay of 110 ps, in good agreement with ring oscillator data for 10-μm SDFL NOR gates. The observed dynamic switching energy varied over the 0.25–0.45-pJ/gate range, depending on the bias conditions and wafer pinchoff voltage. Power dissipation ranged from 45 to 145 mW for the 3-stage dividers.

In understanding the significance of these results, it is especially important to recognize that the DFF was chosen for the ripple divider because of its general usefulness as a building block for more sophisticated logic circuits, not because it provides a particularly high-speed frequency divider. Other circuit approaches, such as a complementary-clocked master–slave divider are architecturally superior as microwave frequency dividers, since the same 110-ps propagation delay would, in that circuit, yield a maximum clock frequency of nearly 4 GHz, albeit at the expense of more difficult clocking requirements. The main accomplishment of the DFF $\div 8$ measurements is the demonstration of very low effective gate propagation delays under fan-out and fan-in of 3 loading conditions, in a circuit with critical timing paths.

In addition, larger MSI circuits including an 8-input data multiplexer containing 64 gates have been evaluated.

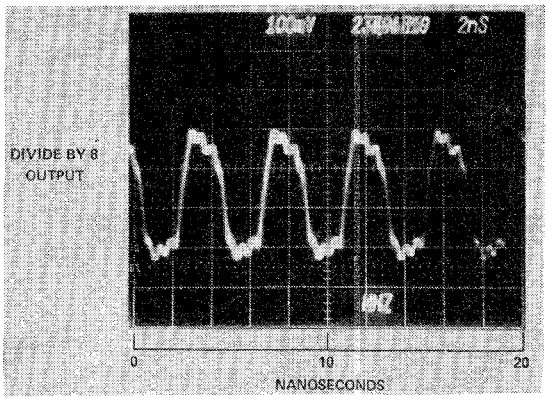

Fig. 2. Divide by 8 output of 3-stage DFF binary ripple divider operating at a 1.9-GHz clock input frequency.

This circuit would be useful, for example, for parallel-to-serial conversion or a high-speed gigabit data transmission link. A logic diagram of this circuit is shown in Fig. 3, and an SEM photograph of a multiplexer chip is shown in Fig. 4 of this circuit. The size, excluding probe pads, is only 0.77×0.54 mm. This circuit utilizes a 3-stage DFF implemented synchronous counter as an address generator for the multiplexer gate array. The data output of the multiplexer is latched using another DFF stage to prevent glitching. Operation of this multiplexer has been achieved at a clock frequency of 1.1 GHz. Fig. 5 shows the output of the multiplexer at 700 MHz with inputs 3 and 6 biased at V_{DD} and all others at ground. This results in the repetitive bit pattern shown when the multiplexer is clocked. The output of the multiplexer at a 1.1-GHz clock rate with a single input biased at V_{DD} is shown in Fig. 6. Power dissipation of the multiplexer circuits varied from 75 mW to 375 mW for wafers with pinchoff voltages of 0.5 V and 1.45 V, respectively.

A 1-input to 8-output data demultiplexer containing 60 gates was also fabricated and evaluated. The circuit design used for this device is quite similar to the data multiplexer, and could be applied at the receiving end of a high-speed gigabit data link. A synchronous counter provides the address for selecting 1 out of 8 NOR gates sharing a common data input. Operation of this circuit has also been demonstrated at a clock frequency of 1.1 GHz. A waveform, measured on a sampling oscilloscope, for an output of the demultiplexer with the input biased at V_{DD} is shown in Fig. 7. Here a clock frequency of 1.025 GHz was used. Bandwidth of the measurement system was limited to 900 MHz by the Tektronix FET probe used to buffer the output of the demultiplexer. The demultiplexer was also evaluated at low clock frequency using a 250-MHz generator as a data source as shown in Fig. 8. In this figure, both clock input and data output are displayed. An output burst is seen every 8 clock cycles as expected.

An MSI combinatorial circuit consisting of a 3×3-bit parallel multiplier, with a total gate count of 75, was also fabricated using the planar SDFL approach, and evaluated for high-speed operation. Very high speed multipliers are an important part of many signal processing and computer systems, because often the data rate is

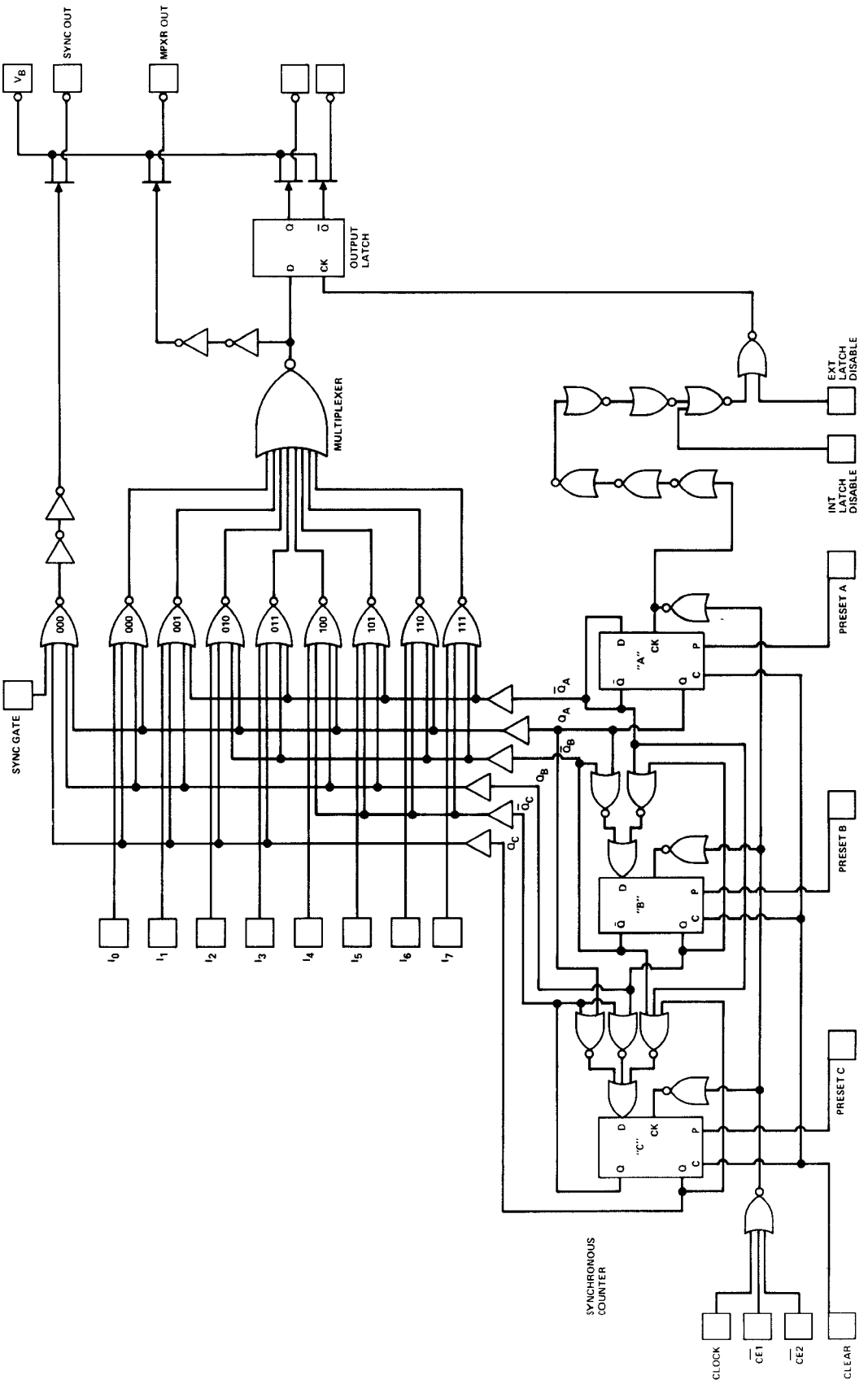

Fig. 3. Logic diagram of the 8-input multiplexer.

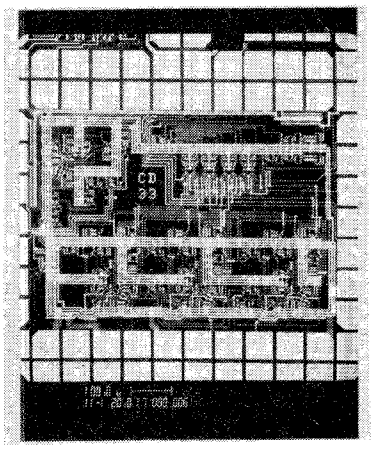

Fig. 4. SEM photograph of an 8-input data multiplexer chip containing 64 gates.

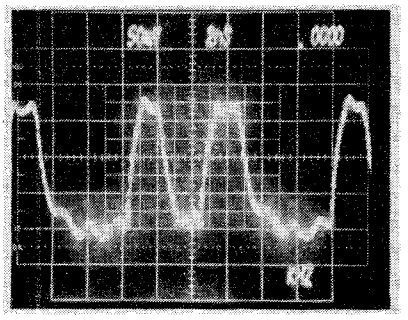

Fig. 5. Multiplexer output waveform with inputs 3 and 6 biased at V_{DD} and 700-MHz clock frequency.

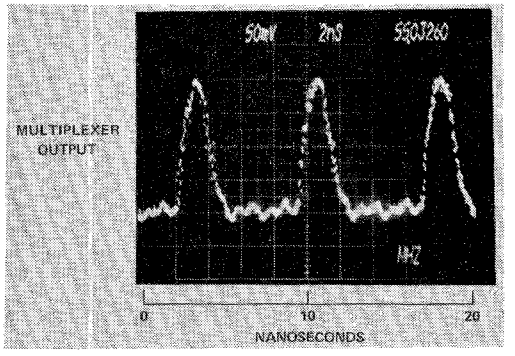

Fig. 6. Multiplexer output waveform with single input biased at V_{DD} and 1.1-GHz clock frequency.

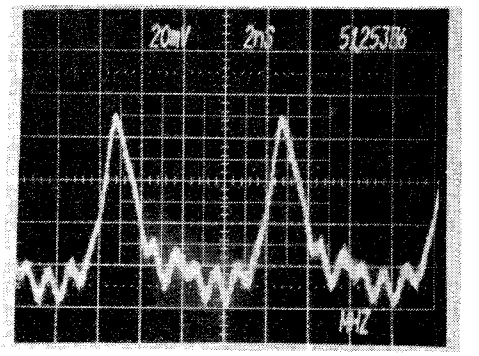

Fig. 7. Demultiplexer output at 1.025-GHz clock frequency.

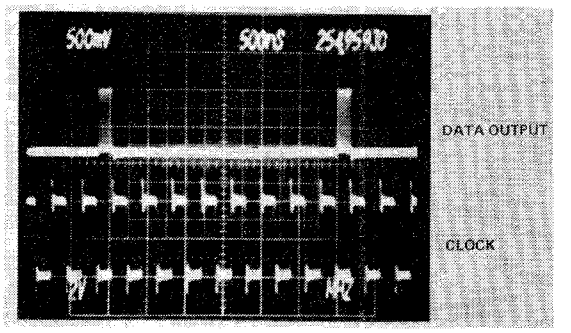

Fig. 8. Demultiplexer output and clock input using 250-MHz data source.

determined by the time required to perform a complex multiplication. In a $N \times N$ parallel or array multiplier, $N(N-2)$ full adders and N half adders are used to sum the partial product bits in $(N-1)$ sum delays plus $(N-1)$ carry delays. Thus, in a large parallel multiplier, the speed will be dominated by the full adder cell propagation delay.

In this study, a NOR-implemented full adder was utilized as shown in Fig. 9. This results in a $3\tau_d$ delay for the sum and a $2\tau_d$ delay for the carry and requires 12 gates. The full-adder and half-adder cells are interconnected as shown in Fig. 10, where F stands for a full-adder cell and H for a 5-gate half-adder cell. For the $N=3$ case, 3 half- and 3 full-adders are required. Partial products are formed by NOR gates connected to the inverted input bits. An SEM photograph of the planar SDFL realization of this circuit is shown in Fig. 11. The size of this circuit, excluding probe pads, is 0.54×0.77 mm.

Proper operation of the 3×3-bit multiplier was observed under low-speed and high-speed modes of evaluation. A specific input code ($111 \times 10S = S\bar{S}\bar{S}\bar{S}SS$) was chosen to demonstrate the correct operation, where a pulse input S at a clock frequency of 200 Hz is applied to the A_0 input as shown on the top of Fig. 10. Upon this A_0 pulse input, the product outputs P_2, P_3, and P_4 will display the inversion of S, and the other outputs will assume the waveform of A_0, which can be seen in Fig. 12. The total power dissipation for the 3×3 multiplier was 31.5 mW with $V_{DD} = 1.77$ V and $V_{ss} = -0.94$ V. This corresponds to a power dissipation of 420 μW/gate.

To evaluate the propagation delay per gate or the multiply time, an optional NOR control gate and a feedback loop from P_5 (the most significant bit of the product) to A_0 (the least significant bit of the multiplicand) has been included to allow operation in a ring oscillator-like mode. An oscillating frequency of $1/18\tau_d$ is expected for the A_0 to P_5 delay path through the multiplier. Fig. 13 shows the output waveform of the multiplier operating in the ring oscillator mode with input words $B = 111$ and $A = 100$. An oscillation frequency of 323 MHz was obtained, corresponding to a propagation delay of 172 ps/gate, with a speed–power product of $P_D\tau_d = 128$ fJ/gate. Devices from lower pinchoff voltage wafers operated at $f_0 = 246$ MHz for a gate delay of 225 ps and a $P_D\tau_d = 95$ fJ/gate. The highest speed devices would therefore yield a complete 3×3 multiplication in approximately 1.5 ns.

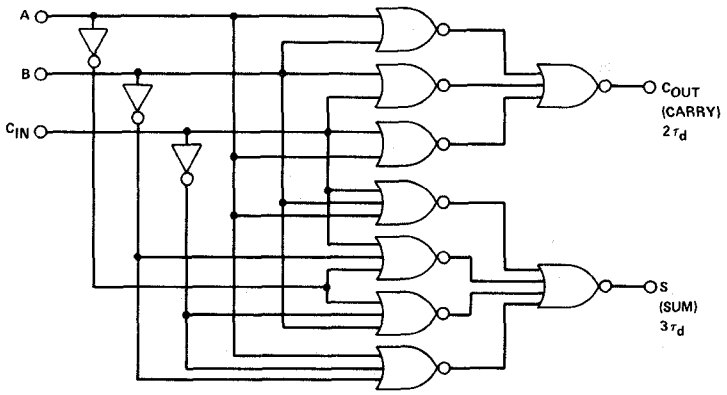

Fig. 9. Full adder cell for array multiplier as implemented with 12 SDFL NOR gates. Carry delay is 2 τ_d and sum delay is 3 τ_d where τ_d is the basic NOR gate delay.

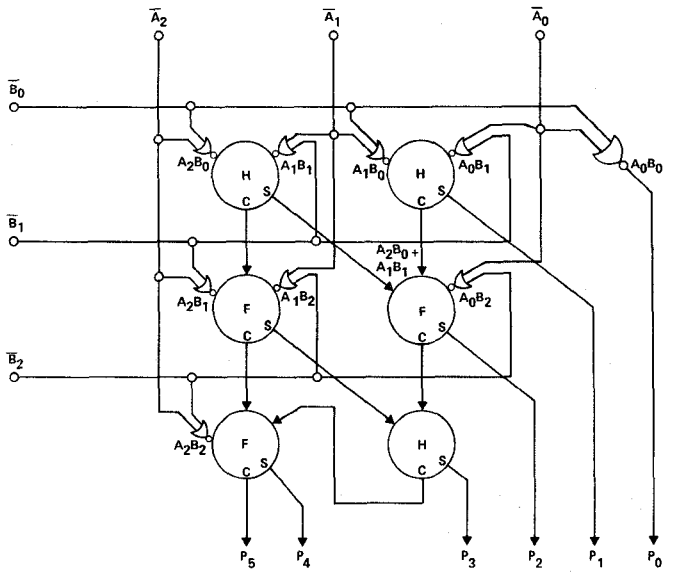

Fig. 10. Logic diagram of 3×3-bit parallel multiplier. Full adder cells (*F*) are as shown in Fig. 9. Half-adder cells (*H*) are implemented with 5 SDFL NOR gates. Input inverters, output buffers, and on-chip feedback connections are not shown.

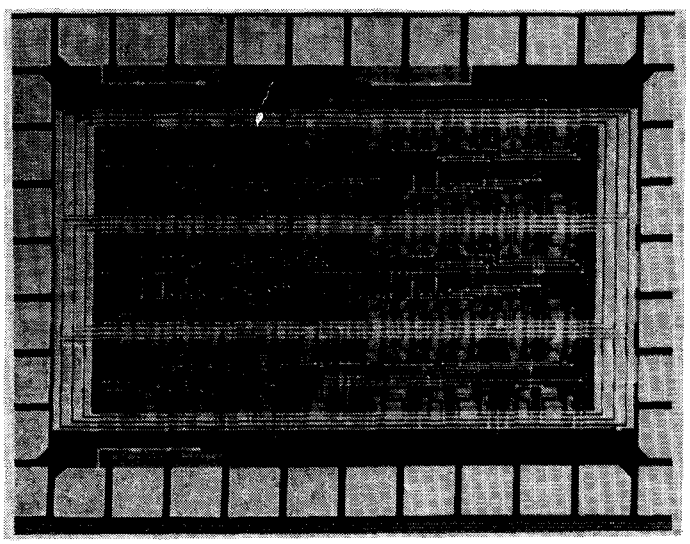

Fig. 11. Photograph of 3×3 multiplier.

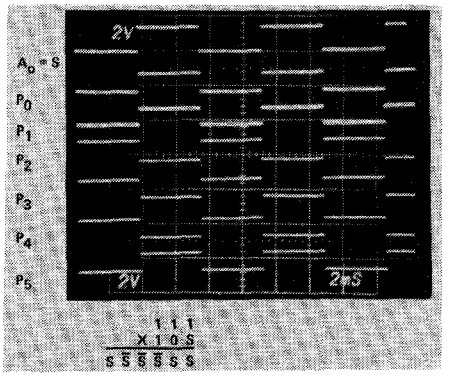

Fig. 12. Outputs of 3×3 multiplier at low-frequency test. The input code is $111 \times 10S = \overline{SSSSSS}$, where S is a square-wave input supplied to A_0.

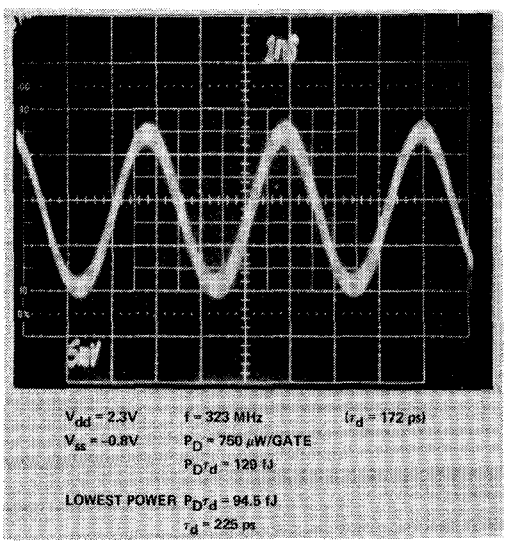

Fig. 13. Output from 3×3 multiplier operating in the ring oscillator mode at 323 MHz. This corresponds to a 172-ps gate delay and 128-fJ/gate dynamic switching energy.

It is possible to extrapolate the performance observations on the 3×3 multiplier to project performance of anticipated future 8×8 parallel multipliers, because the multiply time is most directly linked to the performance of the individual full-adder cells. Thus circuit size increases do not significantly increase gate delays for this particular circuit architecture. For a $\tau_d = 172$ ps, an 8×8-bit multiply could be completed in approximately 6 ns for the simple array architecture. Chip dissipations as low as 300 mW might be achieved with an average power dissipation per gate of 420 μW. This would represent a significant improvement over state-of-the-art commercially available 8×8 silicon parallel multipliers which provide 60 ns internal multiply times at chip-power dissipations over 1 W.

IV. Conclusion

The Schottky diode FET logic circuit design has been successfully implemented in GaAs by means of a planar fabrication approach. Applications of this technique have progressed beyond the early feasibility stages as evidence by the demonstration of MSI digital circuits with up to 75

gates/chip. High-speed performance was demonstrated on binary ripple dividers, an 8-channel data multiplexer and demultiplexer and a 3×3-bit parallel multiplier. The favorable speed–power products achieved indicate that the high-density planar SDFL circuit approach is suitable for extension into the LSI range of complexity where many interesting gigabit microwave data and frequency control circuit applications can be addressed.

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An *E*-Beam Fabricated GaAs *D*-Type Flip-Flop IC

MAURICE GLOANEC, GÉRARD NUZILLAT, CHRISTIAN ARNODO, AND MICHEL PELTIER

***Abstract*—A first generation of monolithic digital IC's using normally-on type GaAs MESFET's with 1.2-μm gate length was initially developed. This technology leads to logic gates with propagation delays in the range 130–170 ps. It was applied to the fabrication of an edge-triggered *D*-type flip-flop IC whose performance is presented: minimum data pulsewidth (350 ps), maximum toggle frequency (up to 1.6 GHz), data input sensitivity. An improved technology intended for higher speeds is now under development. It utilizes direct-writing *E*-beam lithography to delineate 0.75-μm gate length devices with extremely high alignment accuracy. This fabrication process leads to 61 ps (4 pJ) or 68 ps (2 pJ) propagation delays measured on a dual-ring oscillator test circuit. Recent advances in N/N^- epitaxial deposition techniques make these performances very uniform and satisfactorily reproducible. *D*-type flip-flop IC's have been fabricated with this new technology using a reduced (−1 to −1.5 V) pinchoff voltage value. Stable *D*-type operation up to 3-GHz clocking frequencies has been experimentally observed with a corresponding speed–power product of 2.6 pJ/gate.**

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I. Introduction

THE EARLY efforts to fabricate gallium-arsenide integrated circuits (IC's) had successfully demonstrated the potential of the metal–semiconductor field-effect transistors (MESFET) in developing high-performance digital IC's [1]. Switching times under 100 ps have been achieved with logic gates fabricated from 1-μm gate length depletion-mode devices (so-called normally-on MESFET's) by a two-stage circuit design now named buffered-FET logic (BFL), or drain-merging logic [2]. More recently, propagation delays as low as $t_{pd}=34$ ps have been measured from BFL ring oscillators designed with 0.5-μm gate length [3].

The main disadvantage of this GaAs approach is certainly the relatively high power dissipation, typically

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